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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/506,826	09/07/2004	Shinji Isokawa	10921.246USWO	8911

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EXAMINER	
MAGEE, THOMAS J	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 06/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/506,826	ISOKAWA ET AL.	
	Examiner	Art Unit	
	Thomas J. Magee	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-11 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-11 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 09072004.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections – 35 U.S.C. 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 – 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perez et al. (US 6,847,103 B1) in view of Oida et al. (US 6,291,274 B1).

3. Regarding Claim 1, Perez et al. disclose a semiconductor device comprising an insulating substrate (76) (Figure 7) (Col. 5, line 54 - 55) having an obverse surface formed with a square die pad (22) (Figure 2) made of metal film (Col. 3, line 61 through Col. 4 line 10) and a pair of electrode terminals (16) made of a metal film, a rectangular semiconductor chip (56) (Col. 5, lines 20) bonded to the obverse side of the die pad with a die bonding material (58) (Col. 5, lines 17 – 20) and a molded portion (66) (Col. 5, lines 30 – 36) made of synthetic resin for packaging the semiconductor chip.

wherein a narrow patterned conductor made of a metal film (24) (Figure 2) is provided between the die pad and one of the electrode terminals (16) to integrally connect the pad and the electrode.

Perez et al. do not disclose that the semiconductor chip comprises an LED chip or that the molded portion is light permeable. Oida et al. disclose that the semiconductor chip is an LED (Col. 18, lines 1 – 4) and that the molded resin is light permeable (Col. 9, lines1 – 2). It would have been obvious to combine Oida et al. with Perez et al. to obtain a package of versatility for mounting an LED with required transparent molding.

Further, Perez et al. do not disclose that the rectangle of the die pad has a length and a width which are 0.50 to 1.50 times the length and width of the rectangle of the semiconductor chip, respectively. Perez et al. do disclose that the die pad is square (Figure 2). Sizing of dimensions of die pad areas in the art of semiconductor manufacturing processing are subject to routine experimentation and optimization to achieve the desired package quality during device fabrication. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the pad dimensions within the range claimed in order to form a high quality packaging structure.

4. Regarding Claim 2, Perez et al. disclose that the die pad (22) (Figure 2) has a side surface integrally formed with a narrow extension (24) projecting outward from the die pad.

5. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perez et al. in view of Oida et al., as applied to Claims 1 and 2, and further in view of Kwan et al. (US 6,872,661 B1).

6. Regarding Claim 3, Perez et al. do not disclose that the die pad is formed with a recess of a size insufficient to receive the semiconductor chip. Kwan et al. disclose (Figure 1H) a patterned metal film (202) containing recesses and used as a die pad layer, wherein the recesses are of a size insufficient to receive the semiconductor chip.. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Kwan et al. with Perez et al. to obtain a device package with reduced maximum stresses caused by the difference in thermal expansion between the die and die attach pads (Kwan et al., Col. 5, lines 37 – 42).

7. Regarding Claim 4, Perez et al. disclose that the die pad (22) (Figure 2) has a side surface integrally formed with a narrow extension (24) projecting outward from the die pad.

Perez et al. do not disclose that the die pad is formed with a recess of a size insufficient to receive the semiconductor chip., Kwan et al. disclose (Figure 1H) a patterned metal film (202) containing recesses and used as a die pad layer wherein the recesses are of a size insufficient to receive the semiconductor chip. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Kwan et al. with Perez et al. to obtain a device package with reduced maximum stresses caused by the difference in thermal expansion between the die and die attach pads (Kwan et al., Col. 5, lines 37 – 42).

8. Claims 5, 6, 8, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perez et al..

9. Regarding Claim 5, Perez et al. disclose a semiconductor device comprising an insulating substrate (76) (Figure 7) (Col. 5, line 52) having an obverse surface formed with a square die pad (22) (Figure 2) made of metal film (Col. 3, line 61 through Col. 4 line 10) and a pair of electrode terminals (16) made of a metal film, a square semiconductor chip (56) viewed in plan and bonded to the obverse side of the die pad with a die bonding material (58) (Col. 5, lines 17 20) and a molded portion (66) (Col. 5, lines 30 – 36) made of synthetic resin for packaging the semiconductor chip.

Perez et al. do not explicitly disclose that the die pad is circular, but do disclose that the pad can be polygonal, and will approach a circular shape in plan. Further, Perez et al. do not disclose the diameter of the "circular" die pad or that the diameter approximates the diagonal dimension of the semiconductor chip. However, the sizing of chip size for package design to fulfill packaging requirements is routine in the art and subject to routine experimentation and optimization. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the chip size in the range as claimed to form an efficient and reliable package design.

wherein, a narrow patterned conductor (24) made of a metal film (Col. 3, line61 through Col. 4, line 10) is provided between the die pad (3A) and one of the electrode terminals (3C) to integrally connect the die pad and terminal to each other.

10. Regarding Claim 6, Perez et al. do not disclose that the diameter of the die pad is 0.6 to 1.5 times the diagonal dimension of the semiconductor chip. However, the sizing of pad size for package design to fulfill packaging requirements is routine in the art and subject to routine experimentation and optimization. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the pad size in the range as claimed to form an efficient and reliable package design.

11. Regarding Claim 8, Perez et al. disclose that the paired electrode terminals (24) are arranged, as viewed in plan (Figure 2), on a generally straight line with the die pad (22), interposed therebetween, the narrow patterned conductor (24) being arranged to extend from a circumference of the die pad at a position deviating by 45 degrees from the line of the electrode terminals.

12. Regarding Claim 11, Perez et al. disclose a semiconductor device comprising a die pad (22) and a pair of electrode terminals (16) made of metal plate (film) (Col. 3, line 61 through Col. 4 line 10), a semiconductor chip that is square (Col. 5, lines 16 – 18) as viewed in plan, and bonded to the die pad with a die bonding material (58), and a a molded portion (66) made of synthetic resin (Col. 5, lines 17 – 18) for packaging the semiconductor chip, wherein a narrow patterned conductor made of a metal film (24) (Figure 2) is provided between the die pad and one of the electrode terminals (16) to integrally connect the pad and the electrode.

Further, Perez et al. do not explicitly disclose that the die pad is circular, but do disclose

that the pad can be polygonal (Col. 5, line 67), and will approach a circular shape in plan. Further, Perez et al. do not disclose the diameter of the "circular" die pad or that the diameter approximates the diagonal dimension of the semiconductor chip. However, the sizing of chip size for package design to fulfill packaging requirements is routine in the art and subject to routine experimentation and optimization. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the chip size in the range as claimed to form an efficient and reliable package design.

13. Claims 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perez et al., as applied to Claims 5, 6, 8, and 11, and further in view of Oida et al.

14. Regarding Claim 7, Perez et al. do not disclose that the semiconductor chip comprises an LED chip or that the molded portion is light permeable. Oida et al. disclose that the semiconductor chip is an LED (Col. 18, lines 1 – 4) and that the molded resin is light permeable (Col. 9, lines1 – 2). It would have been obvious to combine Oida et al. with Perez et al. to obtain a package of versatility for mounting an LED with required transparent molding.

15. Regarding Claim 9, as stated for Claim 8, Perez et al. disclose that the paired electrode terminals (24) are arranged, as viewed in plan (Figure 2), on a generally straight line with the die pad (22), interposed therebetween, the narrow patterned conductor (24) being arranged to extend from a circumference of the die pad at a position deviating by 45 degrees from the line of the electrode terminals. However, Perez et al. do not disclose that the semiconductor chip com-

prises an LED chip or that the molded portion is light permeable. Oida et al. disclose that the semiconductor chip is an LED (Col. 18, lines 1 – 4) and that the molded resin is light permeable (Col. 9, lines1 – 2). It would have been obvious to combine Oida et al. with Perez et al. to obtain a package of versatility for mounting an LED with required transparent molding.

16. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Perez et al. as applied to Claims 5, 6, 8, and 11, and further in view of Kwan.

17. Regarding Claim 10, Perez et al. do not disclose that the die pad is formed with a recess of a size insufficient to receive the semiconductor chip. Kwan et al. disclose (Figure 1H) a patterned metal film (202) containing recesses and used as a die pad layer, wherein the recesses are of a size insufficient to receive the semiconductor chip.. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Kwan et al. with Perez et al. to obtain a device package with reduced maximum stresses caused by the difference in thermal expansion between the die and die attach pads (Kwan et al., Col. 5, lines 37 – 42).

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Conclusions

16. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(571) 272 1658.** The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the

examiner's acting supervisor, **Stephen Loke**, can be reached on **(571) 272-1657.** The fax number for the organization where this application or proceeding is assigned is **(703) 872-9306.**

Thomas Magee
June 18, 2005

Steven Loke
Primary Examiner